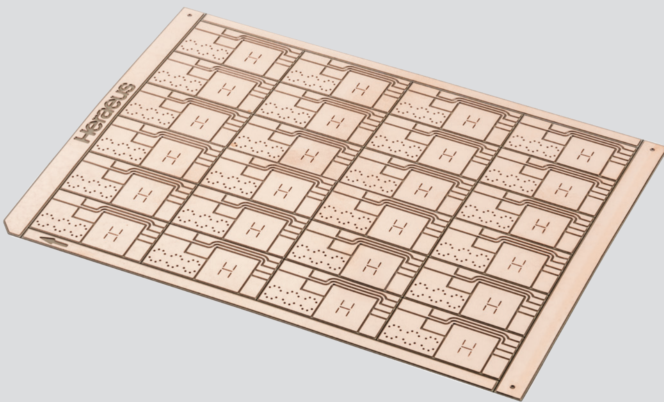
Heraeus

Electronics

Condura®.Extra

Metal Ceramic Substrates Condura.extra DPIS(1)



ZTA DCB facts

- ZTA ceramic Al_2O_3 (9 - 14%)
  Thicknesses(2): 0.25mm/0.32 mm
- Direct Copper Bonding Cu-OFE
  Thicknesses(2): 0.2 mm/0.3 mm
- Single unit or master card size 7 " x 5 " (usable area)
- Surface finish: bare Cu, Ni, Ni/Au, Ag (partial Ag on request)

Key properties

- Dimples (stress relief)
- DMC (Data Matrix Code)

Process features:

- Grinding surface treatment
- Laser technology
- US Scan
- AOI (Automatic Optical Inspection)

Key features

- Higher reliability version and economic version available

Main properties substrate (DCB)

	Rating	Unit
Thermal conductivity @ 20 °C	≥	22W/m.K
Bending strength	600 - 650	MPa
Die electric strength	≥	20kV/mm

*Picture: substrate layout by courtesy of Fraunhofer IISB
(1) Development Product Information Sheet, preliminary values
(2) Different material combinations on request

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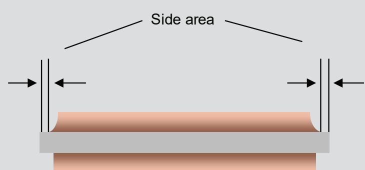
Design Rules DPIS[1]

Material properties raw Al_2O_3[3]

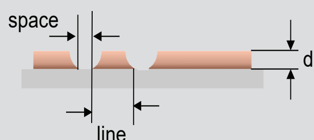
	Rating	Unit
Density	> 3.95	g/cm^3
Electrical resistivity	≥ 10^{14}	Ohm·cm

Copper free area



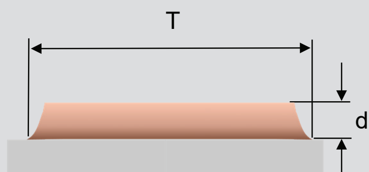
Thickness Cu [mm]	Min. side area [mm]
0.20	0.20
0.30	0.25

Structuring



Thickness Cu [mm]	Min. space [mm]	Min. line [mm]
0.20	0.40	0.40
0.30	0.50	0.50

Etching tolerance



Tolerance length & width [mm]	Thickness Cu [mm]
$T_{typ.}$ = ± 0.15	d = 0.2
$T_{typ.}$ = ± 0.20	d ≤ 0.3
$T_{typ.}$ = ± 0.20	d ≤ 0.4

(1) Development Product Information Sheet, preliminary values
(3) Depends on supplier

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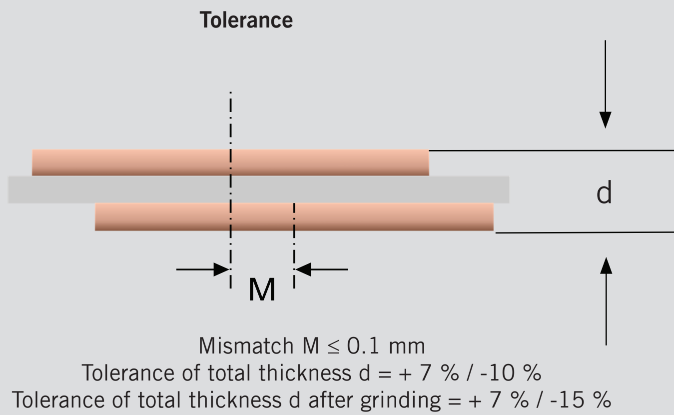
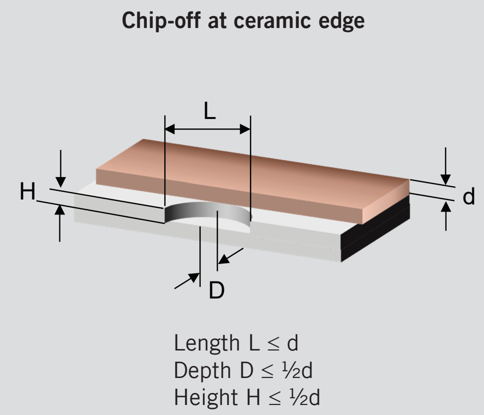
Tolerance and chip off

Tolerance



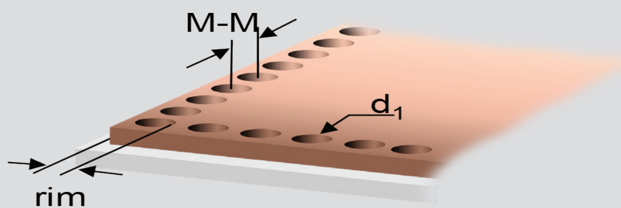
Mismatch M ≤ 0.1 mm
Tolerance of total thickness d = + 7 % / -10 %
Tolerance of total thickness d after grinding = + 7 % / -15 %

Chip-off at ceramic edge



Length L ≤ d
Depth D ≤ ½d
Height H ≤ ½d

Dimple structure



Thickness Cu [mm]	Dimple area rim [mm]	Dimple diamter d_1 [mm]	Dimple pitch M-M [mm]
0.20			
0.30			
0.40			

Dimensions

General dimensions	Rating (mm)
Master card	138 x 190.5
Max. usable area	127 x 178
Minimum dimension for ceramic thickness ≤ 0.32 mm	10 x 10 (smaller on request)

Tolerances of single parts	Rating (mm)
Ceramic thickness 0.32 mm	+ 200 µm - 50 µm

Warpage behavior depends on specific layout, single part size and material combination and can only be specified after initial sample preparation.

Surface plating

Plating Method	Thickness (um)
Electroless Ni	3 - 7 (9% ± 2 % P)
Electroless NiAu	Ni 3 - 7 (9 % ± 2 % P)
	Au Class 1: 0.01 - 0.05
	Au Class 2: 0.03 - 0.13
Ag	0.2 - 0.3

(1) Development Product Information Sheet, preliminary values

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Metal & hole properties

Roughness	
Rmax = 50 µm	
Ra ≤ 3.5 µm	Ra ≤ 1 µm
Rz ≤ 24 µm	Rz ≤ 16 µm

Different roughness by request

Minimum hole diameter
d_{hole} = 1 mm

Electrical conductivity raw copper
$G_{Cu} = 58 \cdot 10^6$ S/m

Thickness Cu	Copper peeling Strength
0.30mm	> 4 N/mm

HET Academy
R&D Application Center

Besides offering Assembly Materials, Bonding Wires and Metal Ceramic Substrates, Heraeus Electronics provides matching material solutions and R&D oriented partnerships to create individual solutions.

Application conditions and assembly optimization

Thermal shock test cycles
-55 °C up to +150 °C
Information upon request

Customized surface for assembly process

Optimization of surface and assembly process parameters available or in developement cooperation for:

- Sintering
- Solder wetting
- Heavy wire bondability

12.2021, Layout: CF

Heraeus Electronics offers:

- Reliable IATF 16949 certified supply of:
  - ✓ Condura®.prime AMB-Si_3N_4 (active metal brazed Si_3N_4)
  - ✓ Condura®.extra DCB-ZTA (zirconia-toughened alumina)
  - ✓ Condura®.classic DCB-Al_2O_3 (direct copper bonded Al_2O_3)
- Condura® + for example:
  - ✓ Engineering Services (Simulation, Prototype Design & Assembly, Testing and Qualification, Material Analysis)
  - ✓ Pre-applied sinter / solder
- To be your competent **one-stop materials solutions partner**!

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(1) Development Product Information Sheet, preliminary values